REMARKS

Claims 1 and 3-12 have been amended. Claim 2 has been canceled. Claims 1 and 3-12 are currently pending in this application. Applicant reserves the right to pursue the original and other claims in this and other applications. Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

Claims 6 and 11 stand objected to for informalities. Claims 6 and 11 have been amended to correct for antecedent basis, as suggested by the Examiner. As such, Applicant submits that claims 6 and 11 are in condition for allowance and request that the objection be withdrawn.

Claims 1, 2, 4, 11 and 12 stand rejected under 35 U.S.C. § 102(a)/(e) as being anticipated by Nakatani et al. (U.S. Appl. Pub. 2005/0051899) ("Nakatani"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 1 recites a semiconductor device including a "semiconductor substrate," a "polysilicon pattern formed on said semiconductor substrate via an insulation film, wherein said polysilicon pattern includes at least one doped gate electrode and at least one doped resistance element," an "interlayer insulation film formed on said semiconductor substrate so as to cover said polysilicon pattern," a "first silicon nitride film formed on said interlayer insulation film," a "metal interconnection layer pattern formed on directly said first silicon nitride layer" and a "second silicon nitride film formed directly on a top surface and sidewall surfaces of said metal interconnection layer pattern." Further, the "metal interconnection layer pattern is not an uppermost interconnection layer." Claim 11 recites a method of forming a semiconductor device similar to that of claim 1.

The claimed invention allows a metal interconnection pattern to be formed freely over the substrate while still maintaining control over the resistance value of the polysilicon resistance pattern as desired. Specification, pg. 39, lines 2-12. This is because the first and second nitride films help to regulate the amount of hydrogen incorporated into a patterned polysilicon layer.

Nakatani does not disclose, teach or suggest that the "polysilicon pattern includes at least one doped gate electrode and at least one doped resistance element." Nakatani merely discloses a polysilicon interconnect and does not disclose that this polysilicon interconnect is a doped gate electrode or a doped resistance element. In fact, in order for a silicon layer to act as an interconnection, then resistance must be low.

Accordingly, claims 1 and 11 are allowable over Nakatani. Claim 4 depends from claim 1 and is allowable along with claim 1. Claim 12 depends from claim 11 and is allowable along with claim 11.

Applicant additionally notes that claims 4 and 12 are also allowable over Nakatani, because Nakatani does not disclose the alleged first and second silicon nitride films being removed from any portion of the structure, which is required by claims 4 and 12. Accordingly, claims 4 and 12 are further allowable for this reason in addition to those discussed above.

Applicant requests that the rejection of claims 1, 4, 11 and 12 be withdrawn and the claims allowed.

Claim 3 stands rejected under 35 U.S.C. § 103(a)[1] as being unpatentable over Nakatani in view of Oku (U.S. Patent No. 5,812,364) ("Oku"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 3 depends from claim 1, which is allowable over Nakatani for at least the reasons discussed above. Oku is relied upon as disclosing that the nitride films may have different thicknesses (Office Action, pg. 4), and does not remedy the deficiencies of Nakatani as to claim 1. As such, Applicant respectfully submits that claim 3 is allowable over the cited combination. Applicant requests that the rejection of claim 3 be withdrawn and the claim allowed.

[1] Applicant notes that although the Office Action states that claim 3 is rejected under 35 U.S.C. § 102(a)/(e), Applicant assumes the rejection is under 35 U.S.C. § 103(a) since it is based on a combination of references.

Claims 1, 2, 4-7, 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shimizu (EP-1310998-A2) ("Shimizu") in view of Nakatani. This rejection is respectfully traversed and reconsideration is respectfully requested.

Applicant respectfully submits that there is no teaching, suggestion, or motivation to one of ordinary skill in the art to combine Shimizu with Nakatani to arrive at the claimed invention. The Office Action states that the motivation to combine is the "desirability to passivate and protect the metal interconnect layer patter with the barrier silicon nitride films having an excellent in corrosion resistance." Office Action, pg. 6. Applicant respectfully disagrees. Applicant notes that the nitride layers of Nakatani are put in place to avoid corrosion of the metal interconnect layer. Nakatani, ¶[0055]. This would be necessary only on an uppermost metal interconnect layer (and one skilled in the art would not be motivated to add these layers to metal interconnect layers which are not the uppermost). Thus if Nakatani were to be combined with Shimizu, the claimed invention would not result.

Accordingly, Applicant respectfully submits that claims 1 and 11 are allowable over the cited combination. Claims 4-7 depend from claim 1 and are allowable along with claim 1. Claim 12 depends from claim 11 and is allowable along with claim 11. Applicant requests that the rejection of claims 1, 4-7, 11 and 12 be withdrawn and the claims allowed.

Claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shimizu in view of Nakatani and further in view of Itoh (U.S. Appl. Pub. 2002/0180453) ("Itoh"). This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 8-10 contain limitations which are similar to those in claim 1, which is allowable over Shimizu in view of Nakatani for at least the reasons discussed above. Itoh is relied upon as disclosing a "semiconductor device, in which the output voltage of the voltage divider ... is being adjustable by disconnection of a fuse element" (Office Action, pg. 8), and does not remedy the deficiencies of the Shimizu/Nakatani combination with respect to claims 8-10. As such, Applicant

submits that claims 8-10 are allowable over the cited combination. Applicant requests that the rejection of claims 1, 2, 4-7, 11 and 12 be withdrawn and the claims allowed.

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shimizu in view of Nakatani and further in view of Oku. This rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 3 depends from claim 1, which is allowable over the Shimizu/Nakatani combination for at least the reasons discussed above. Oku is relied upon as disclosing that the nitride films may have different thicknesses (Office Action, pg. 8), and does not remedy the deficiencies of Shimizu/Nakatani as to claim 1. As such, Applicant respectfully submits that claim 3 is allowable over the cited combination. Applicant requests that the rejection of claim 3 be withdrawn and the claim allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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